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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,335	01/25/2005	Yasushi Inagaki	264533US90PCT	8804
22850	7590	10/05/2006	EXAMINER	
C. IRVIN MCCLELLAND OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			GETACHEW, ABIY	
			ART UNIT	PAPER NUMBER
			2841	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/522,335	INAGAKI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Abiy Getachew	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 25 January 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01/25/2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 01/25/2005.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION*****Claim Rejections - 35 USC § 102***

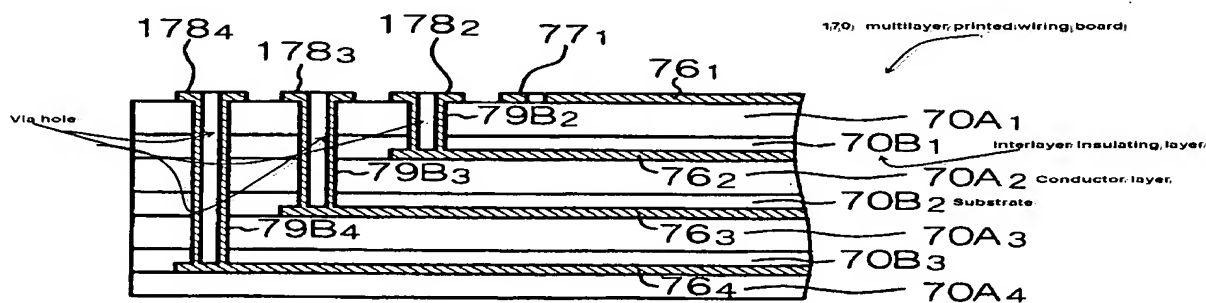
1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Azuma et.al. (US 2004/0108862 A1).

Regarding claim 1 Azuma et.al. Discloses, a multilayer printed wiring board (Figure 23 A Element 170) comprising an interlayer insulating layer ((Figure 23 A Element 70B1) and a conductor layer (Figure 23 A Element 70A2) formed on a core substrate (Figure 23 A Element 70 B2), the conductor layer (Figure 23 A Element 70 A2) being electrically connected through a via hole (Figure 23 A Element 79 B2) wherein a thickness of the conductor layer (Figure 23 A Element 70 A2) on said core substrate (Figure 23 A Element 70 B2) is larger than a thickness of the conductor layer (Figure 23 A Element 70 A1) on the interlayer insulating layer (Figure 23 A Element 70 B1).



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Regarding claim 2 Azuma et.al. discloses, a multilayer printed wiring board (Figure 23 A Element 170) comprising, an interlayer insulating layer (Figure 23 A Element 70B1) and a conductor layer (Figure 23 A Element 70A2) formed on a core substrate (Figure 23 A Element 70B2), the conductor layer being electrically connected through a via hole (Figure 23 A Element 79B2) wherein if a thickness of the conductor layer (Figure 23 A Element 70A2) on said core substrate (Figure 23 A Element 70B2) is  $\alpha_2$  and a thickness of the conductor layer (Figure 23 A Element 70A1) on the interlayer insulating layer (Figure 23 A Element 70B2) is  $\alpha_1$  and  $\alpha_2$  satisfy  $\alpha_2 < \alpha_1 \leq \alpha_4$   $\alpha_2$ . [Column 10 paragraph 2 section 0101]

Regarding claim 3 as applied claim above Azuma et.al. discloses, wherein said  $\alpha_1$  satisfies  $\alpha_2 < \alpha_1 \leq \alpha_4$   $\alpha_2$ . [Column 10 paragraph 2 section 0101]

Regarding claim 4 as applied claim above Azuma et.al. discloses wherein the conductor layer (Figure 23 A Element 70A1) of said core substrate Figure 23 A Element 70B2) is the conductor layer (Figure 23 A Element 70A) for a power supply layer or the conductor layer for an earth. [Column 4 paragraph 2 section 0033, i.e. power supply layer is formed in the internal layer, plate, the first and second electrodes may be formed in part of the ground layer or the power supply layer]

Regarding claim 5 as applied claim above Azuma et.al. discloses, wherein a capacitor is mounted on a surface of the multilayer printed wiring board. [Column 8 paragraph 4 section 0089]

Regarding claim 6 as applied claim above Azuma et.al. discloses a multilayer printed wiring board (Figure 23 A Element 170) comprising, an interlayer insulating layer

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(Figure 23 A Element 70B1) and a conductor layer formed (Figure 23 A Element 70A2) on a core substrate (Figure 23 A Element 70B2), the conductor layer (Figure 23 A Element 70A2) being electrically connected through a via hole (Figure 23 A Element 79 B2) wherein said core substrate (Figure 23 A Element 70B2) is a multilayer core substrate [Column 19 paragraph 3 section 0225] (Figure 23 A Element 70B2) comprising not less than three layers including a thick conductor layer (Figure 23 A Element 70A2) as an inner layer; and the conductor layer (Figure 23 A Element 70A2) as the inner layer and the conductor layer (Figure 23 A Element 70A2) on a surface of said core substrate (Figure 23 A Element 70B2) are the conductor layers (Figure 23 A Element 70A2) for a power supply layer or the conductor layers for an earth.[Column 4 paragraph 2 section 0033]

Regarding claim 7 Azuma et.al. discloses a multilayer printed wiring board (Figure 23 A Element 170) comprising an interlayer insulating layer (Figure 23 A Element 70B1) and a conductor layer (Figure 23 A Element 70A2) formed on a core substrate (Figure 23 A Element 70 B2), the conductor layer (Figure 23 A Element 70 A2) being electrically connected through a via hole (Figure 23 A Element 79B2) wherein said core substrate (Figure 23 A Element 70B2) is a multilayer core substrate (Figure 23 A Element 70B2) comprising not less than three layers including a thick conductor layer as an inner layer, and a conductor layer as an inner layer of said core substrate is the conductor layer as a power supply layer or the conductor layer as an earth and that a conductor layer on a surface [Column 4 paragraph 2 section 0033] layer of said core substrate comprises a signal line. [Column 2 paragraph 3 section 0013]

Regarding claim 8 as applied claim above Azuma et.al. discloses wherein a thickness of the conductor layer (Figure 23 A Element 70A1) on said core substrate (Figure 23 A Element 70B2) is larger than a thickness of the conductor layer (Figure 23 A Element 70A1) on the interlayer-insulating layer (Figure 23 A Element 70B1). [Column 10 paragraph 2 section 0101]

Regarding claim 9 as applied claim above Azuma et.al. discloses wherein the conductor layer (Figure 23 A Element 70A1) as the inner layer of said core substrate (Figure 23 A Element 70B2) is not less than two-conductor layers (Figure 23 A Element 70A1). [Column 1 paragraph 3 section 0004]

Regarding claim 10 as applied claim above Azuma et.al. discloses wherein said core substrate (Figure 23 A Element 70B2) is constituted so that the conductor layer (Figure 23 A Element 70A1) as said inner layer is formed on each surface of an electrically isolated metallic plate through a resin layer and so that said conductor layer (Figure 23 A Element 70A1) on the surface layer is formed outside of the conductor layer (Figure 23 A Element 70A1) as the inner layer through the resin layer. [Column 1 paragraph 2 section 0002]

Regarding claim 11 as applied claim above Azuma et.al. discloses wherein said core substrate (Figure 23 A Element 70B2) comprises a thick conductor layer (Figure 23 A Element 70A1) as the inner layer and a thin conductor layer as the conductor layer on the surface layer. [Column 10 paragraph 2 section 0101]

Regarding claim 12 as applied claim above Azuma et.al. discloses, wherein the conductor layer (Figure 23 A Element 70A1) of said core substrate (Figure 23 A

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Element 70B2) is the conductor layer (Figure 23 A Element 70A1) for power supply layer or the conductor layer for an earth. [Column 4 paragraph 2 section 0033]

Regarding claim 13 as applied claim above Azuma et.al. discloses, wherein a capacitor is mounted on a surface of the multilayer printed (Figure 23 A Element 170) wiring board. [Column 3 paragraph 6 section 0030]

Regarding claim 14 as applied claim above Azuma et.al. discloses, wherein a thickness of the conductor layer on said core substrate is larger than a thickness of the conductor layer on the interlayer-insulating layer. [Column 10 paragraph 2 section 0101]

Regarding claim 15 as applied claim above Azuma et.al. discloses wherein the conductor layer (Figure 23 A Element 70A1) as the inner layer of said core substrate (Figure 23 A Element 70B2) is not less than two conductor layers (Figure 23 A Element 70A1). [Column 1 paragraph 3 section 0004]

Regarding claim 16 as applied claim above Azuma et.al. discloses, wherein said core substrate (Figure 23 A Element 70B2) is constituted so that the conductor layer (Figure 23 A Element 70A1) as said inner layer is formed on each surface of an electrically isolated metallic plate through a resin layer and so that said conductor layer (Figure 23 A Element 70A1) on the surface layer is formed outside of the conductor layer (Figure 23 A Element 70A1) as the inner layer through the resin layer. [Column 1 paragraph 2 section 0002]

Regarding claim 17 as applied claim above Azuma et.al. discloses, wherein said core substrate (Figure 23A Element 70B2) comprises a thick conductor layer (See figure 23 A 70A1) as the inner layer and a thin conductor layer as the conductor layer

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(Figure 23 A Element 70A1) on the surface layer. [Column 10 paragraph 2 section 0101]


### **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abiy Getachew whose telephone number is (571) 272 6932. The examiner can normally be reached on Monday to Friday 8Am to 4:30Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, ENAD G. ELVIN can be reached on (571) 272 1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A.G.  
September 26, 2006

  
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SUPERVISORY PATENT EXAMINER  
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